NMOS

FABRICATION PROCESS

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EVACUATION INSTRUCTIONS FOR TEACHERS

REMINDER : Each teacher is responsible for the orderly and calm evacuation of all students under his care at the time of the incident.

IN THE MAIN CLEAN ROOM:

- ⇨ Evacuate the students by the emergency exit which leads directly into the hall.
- ⇨ Do not go through the airlock again; do not undress.
- ⇨ Exit through the main entrance of AIME.

IN THE PHOTOLITHOGRAPHY ROOM:

- ⇨ Evacuate the students by the emergency exit which leads directly into the corridor.
- ⇨ Do not go through the airlock again; do not undress.
- ⇨ Exit through the main entrance of AIME.

IN ASSEMBLY OR CHARACTERIZATION ROOMS:

- ⇨ Evacuate the students through the emergency exit leading to the green space behind the AIME.
- ⇨ Do not go through the airlock again; do not undress.
- ⇨ Take a tour of AIME.

GATHER ALL STUDENTS AT THE GATHERING POINT IN FRONT OF AIME.

TAKE A CENSUS.

DO NOT REINSTATE THE PREMISES WITHOUT THE ADVICE OF THE PERSONNEL IN CHARGE OF EVACUATION

SECURITY INSTRUCTIONS

LOCATE **THE SAFETY EQUIPMENT**:

- emergency exits
- security showers
- fire extinguishers
- self-contained breathing equipment

WEAR PROTECTIVE GLASSES IS MANDATORY FOR:
- CHEMICAL CLEANING (RCA AND H_2SO_4-H_2O_2)
- ALL WET ATTACKS

TRAINEES ARE **FORBIDDEN** TO TRANSPORT CHEMICALS FROM ONE WORKSTATION TO ANOTHER.

Keep in mind that:

- gloves are compulsory but they do not provide sufficient protection against high temperatures or corrosive products,
- some baths give off noxious vapors, normally drawn in by laminar flow hoods,
- overshoes sometimes make the floor very slippery.

HANDLING INSTRUCTIONS

- Throughout the duration of the process, the quality control of each step must be a permanent concern if we want to achieve a final component in working order, as well as a good performance on the whole. For this purpose, we will use in parallel with the "components" wafer, a control/test wafer (“witness”) which will characterize each step carried out.

- Warning: the wafers boxes must be opened by turning the cover clockwise

- For handling a wafer with a tweezer :

- take advantage of the flat if the wafer is in the box
- pinch at least 5mm from the edge of the wafer to reduce the risk of breakage.

Any wafer coming out of a wet treatment must at the end undergo a rinsing with D.I. water and mechanical drying before being stored in its box.

- A good rinsing must include a change of tweezer, it is necessary to have a second one available and clean all tweezers.

- The tips of the pliers must not be wiped (neither on the gown, nor on paper), they must be rinsed with water and dried with nitrogen.

- The function of the gloves is to protect the components from contamination. Contamination of gloves should also be avoided. They are absolutely not an effective protection against acids.

- The plastic of the boxes cannot withstand temperatures above 250 ° C. In particular, cool down the wafers coming out from oven, for about 20 seconds in the open air.

- Paper is a source of contamination, make minimal use of it.

CLEANROOM ENTRY PROCEDURE

- Leave street clothes and bags in the seminar room.
- Six lockers, lockable, can be used in the SAS for valuables.
- No more than 4 people in the airlock at the same time

Clean room entry:

Lab coat: white : permanent staff
blue: trainees
green: visitors

Overshoes: place the seam inside.
Do not put your foot in the clean part until you have put on your overshoes.

Mob caps: Provision in the wall dispenser.

Gloves: Provision in the wall dispenser. 2 sizes available.

Exit of clean room:

Lab coat/mob caps/goggles: place them in your personal box
Overshoes/gloves: throw them in dedicated trashes.

Recommendations:

- Be careful not to enter the airlock with muddy or wet dress shoes (use the doormat at the entrance of the AIME).
- Limit the number of objects and documents entering the Clean Room (**carbon pencil prohibited**).

PROCESS SHEET: TRANSISTOR WITH POLYSILICON GATE

I- SUBSTRATE CHARACTERIZATION

COMPONENTS WAFERS n° ... :

MATERIAL: Si P type, orientation : (100)

⊂⊃ wafer thickness measurement	e_s =	µm
⊂⊃ 4 probes measurement	V/I =	Ω
⊂⊃ sheet resistance calculation	$R_{\square}$ =	Ω/□
⊂⊃ resistivity calculation	ρ_s =	Ω.cm.
⊂⊃ doping concentration calculation	N_A =	at.cm^{-3}

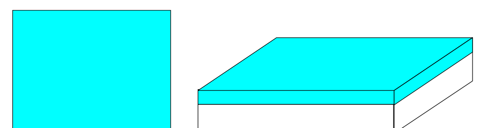
II- MASKING OXIDE

1- Cleaning before Oxidation:

Operations	Conditions
⊂⊃ 1°) Degreasing	Acetone
⊂⊃ 2°) Rinsing	DI water
⊂⊃ 3°) Chemical Oxidation	$H_2SO_4 + H_2O_2$ (1/1) - 2 min
⊂⊃ 4°) Rinsing	DI water
⊂⊃ 5°) SiO_2 etching	BOE HF - 30 s
⊂⊃ 6°) Rinsing	DI water
⊂⊃ 7°) Drying	Spin dryer
⊂⊃ 8°) Washing - Drying	Washer dryer

2- Wet thermal Oxidation: This operation is performed inside oven N° 2-2

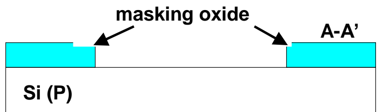
masking oxide
Si (P)
masking oxyde

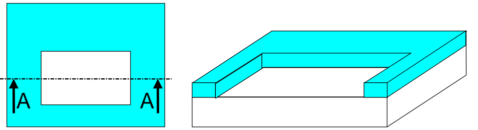


Conditions		
⊂⊃ process also test-wafer 1 and 2		
Temperature	**Duration**	**Flow rates**
⊂⊃ from 800°C to 1100°C	25 min	N_2 = 1 l/min
⊂⊃ 1100°C	35 min	H_2 = 2,3 l/min - O_2 = 1,5 l/min
⊂⊃ 1100°C	30 min	O_2 = 2,2 l/min
⊂⊃ 1100°C	5 min	Ar = 1,5 l/min
⊂⊃ from 1100°C to 800°C	60 min	N_2 = 1 l/min

III- PHOTOLITHOGRAPHY n° 1: "TRANSISTOR OPENING"

This step provides **the channel width « W » of the transistor**.





Supervisor's visa for the continuation of Operations		▼
Operations	**Conditions**	
⊂⊃ 1°) Drying	Hot plate 120°C – 2 min	
⊂⊃ 2°) HMDS Deposit (Adhesion promoter)	Spin coater 4000 rpm - 30 s	
⊂⊃ 3°) Positive photoresist deposit	Resist Shipley S1813 Spin coater 4000 rpm - 30 s	
⊂⊃ 4°) 1st annealing	Hot plate 100°C – 60 s	
⊂⊃ 5°) Alignment - Insolation	Mask n°1 – 5 s	
⊂⊃ 6°) Development	Bath at 20 °C - 25 s	
⊂⊃ 7°) Rinsing	DI water	
⊂⊃ 8°) Drying	Spin dryer	
⊂⊃ 9°) Observation	Optical microscope	☐
⊂⊃ 10°) 2nd annealing	Hot plate 120° C - 45 s	
⊂⊃ **Process test wafer 1**	**Operation n°1 (§ XIX)**	
⊂⊃ 11°) SiO_2 etching	BOE HF : time duration given by test-wafer1	
⊂⊃ 12°) Rinsing	DI water	
⊂⊃ 13°) Drying	Spin dryer	
⊂⊃ 14°) Observation	Optical microscope	☐
⊂⊃ 15°) Resist dissolution	Acetone	

⇨ 16°) Rinsing	DI water
⇨ 17°) Drying	Spin dryer

IV- ORGANIC DECONTAMINATION

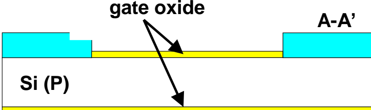
Operations	Conditions
⇨ 1°) Cleaning	$H_2SO_4 + H_2O_2$ - 2 min
⇨ 2°) Rinsing	DI water
⇨ 3°) Drying	Spin dryer

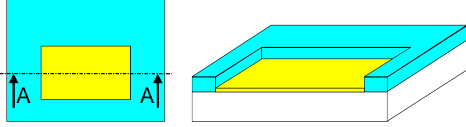
V- CLEANING R.C.A.

This operation aims to prepare the Si - SiO_2 interface before growing the gate oxide, following 5 steps (A' – A – A' – B – C) :

Conditions	
⇨ clean at the same time test-wafer 1, **but not test-wafer 2**	
Operations	**Conditions**
⇨ 1°) Bath A'	Dilute HF – 30 s
⇨ 2°) Rinsing	DI water – 3 min minimum
⇨ 3°) Drying	Spin dryer
⇨ 4°) Bath A	HNO_3 boiling – 10 min
⇨ 5°) Rinsing	DI water – 3 min minimum
⇨ 6°) Bath A'	Dilute HF – 30 s
⇨ 7°) Rinsing	DI water – 3 min minimum
⇨ 8°) Bath B	$NH_4OH + H_2O_2 + H_2O$ boiling - 10 min
⇨ 9°) Rinsing	DI water – 3 min minimum
⇨ 10°) Bath C	$HCl + H_2O_2 + H_2O$ boiling - 5 min
⇨ 11°) Rinsing	DI water – 3 min minimum
⇨ 12°) Drying	Spin dryer

VI- GATE OXIDE



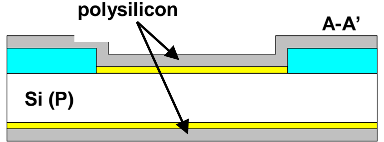


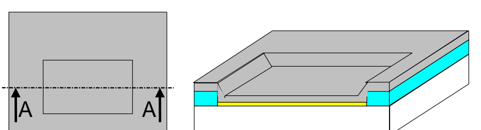
This dry Oxidation is performed in oven N° 2-1 following two steps:

Conditions		
⊂⊃ Process test-wafer 1 also, **but not test-wafer 2**		
Temperature	**Duration**	**Flow rates**
⊂⊃ 1100°C	20 min	O_2 = 2 l/min
⊂⊃ 1100°C	10 min	Ar = 2 l/min

During this operation, continue to characterize the process (*cf* part **XX** "*characterizations*")

VII- POLYSILICON DEPOSIT

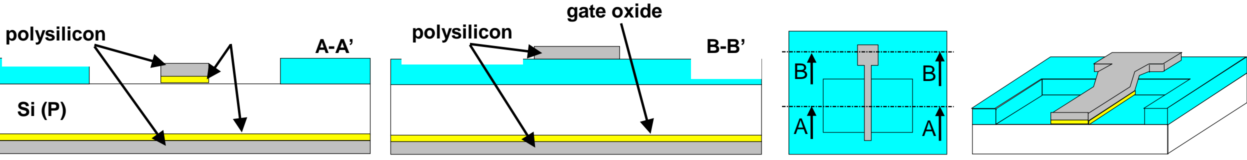




This is performed in the LPCVD (Low Pressure Chemical Vapor Deposition) reactor n°4-3:

Conditions			
⊂⊃ Process also test-wafer 2, **but not test-wafer 1**			
Temperature	**Duration**	**Flow rates**	**Pressure**
⊂⊃ from 400°C to 585°C	20 min	N_2 = 1 l/min	1 Torr
⊂⊃ 585°C	21 min	SiH_4 = 50 cc/min	250 mTorr
⊂⊃ from 585°C to 400°C	20 min	N_2 = 1 l/min (cycles de purge/vide)	1 Torr

VIII- PHOTOLITHOGRAPHY n° 2: "POLYSILICON ETCHING"



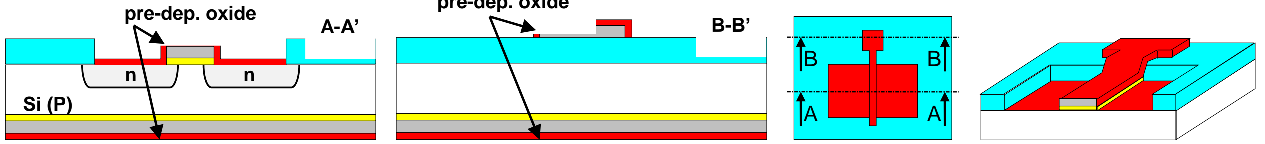
Source and drain are opened for diffusion so the channel **length** “**L**” will be set under the gate.

Operations	Conditions
	Supervisor’s visa for the continuation of Operations ▼
Operations	**Conditions**
⊂⊃ 1°) Drying	Hot plate 120°C – 2 min
⊂⊃ 2°) HMDS deposit (Adhesion promoter)	Spin coater 4000 rpm - 30 s
⊂⊃ 3°) Positive photoresist deposit	Resist Shipley S1813 Spin coater 4000 rpm - 30 s
⊂⊃ 4°) 1st annealing	Hot plate 100°C - 60 s.
⊂⊃ 5°) Alignment - Insolation	Mask n°2 – 5 s
⊂⊃ 6°) Development	Bath at 20 °C - 25 s
⊂⊃ 7°) Rinsing	DI water
⊂⊃ 8°) Drying	Spin dryer
⊂⊃ 9°) Observation	Optical microscope
⊂⊃ 10°) 2nd annealing	Hot plate 120° C - 45 s
⊂⊃ 11°) POLYSILICON ETCHING (components side)	REACTIVE ION ETCHING Flow rate SF_6 : 30 cc/min. Pressure : 0,02 mbar Power RF : 50 W
⊂⊃ 12°) **Do not remove the photoresist**	
⊂⊃ 13°) Observation	Optical microscope
⊂⊃ **Process test-wafer 1**	**Operation n°2 (§ XIX)**
⊂⊃ 14°) SiO2 etching	BOE HF: time duration given by test-wafer1
⊂⊃ 15°) Rinsing	DI water
⊂⊃ 16°) Drying	Spin dryer
⊂⊃ 17°) Observation	Optical microscope
⊂⊃ 18°) Resist dissolution	Acetone + DI water

IX- ORGANIC DECONTAMINATION

Operations	Conditions
⊂⊃ 1°) Cleaning	$H_2SO_4 + H_2O_2$ - 2 min
⊂⊃ 2°) Rinsing	DI water
⊂⊃ 3°) Drying	Spin dryer

X- SOURCE ET DRAIN DIFFUSION (N type)



1- PreDeposit : This operation is performed following 3 steps in oven n°1-1

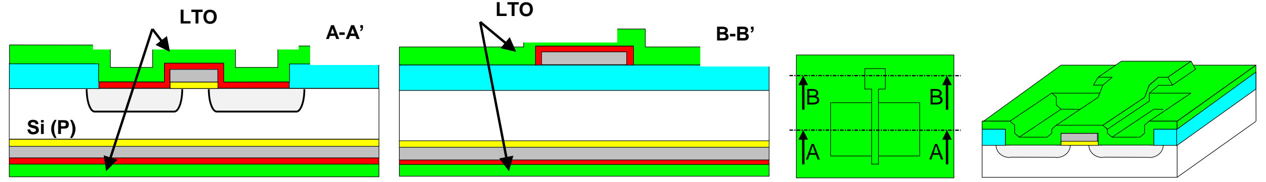
Conditions		
⊂⊃ Process also test-wafer 1 and 2		
Temperature	**Duration**	**Flow rates**
⊂⊃ 1050°C	5 min	N_2 = 2 l/min - O_2 = 0,1 l/min
⊂⊃ 1050°C	10 min	N_2 = 2 l/min - O_2 = 0,1 l/min – $POCl_3$ = 10 mg/min
⊂⊃ 1050°C	6 min	N_2 = 2 l/min - O_2 = 0,1 l/min

2- Drive-in : This operation is performed in oven n°1-1 following these conditions :

Temperature	Duration	Flow rates
⊂⊃ 1100°C	7 min	N_2 = 1 l/min

Supervisor's visa for the continuation of Operations	▼
⊂⊃ Diffusion oxyde e_d thickness measurement on test-wafer 1 - **Operation n°3 (§ XIX)**	
⊂⊃ 4 probes measurement (Oxide etching and V/I)	☐

XI- SiO2 DEPOSIT L.T.O (Low Temperature Oxide)

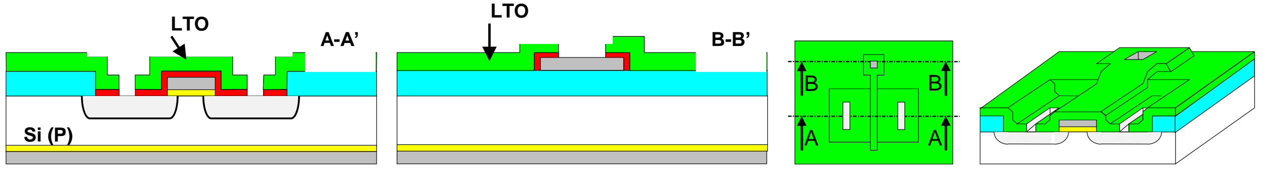


After the source and drain diffusion, an insulating capping layer of SiO_2 L.T.O. (low temperature oxide) is deposited. This operation is performed in oven LPCVD n°3-1 following the conditions:

Conditions			
⊂⊃ Process also test-wafer 2, **but not test-wafer 1**			
Temperature	**Duration**	**Flow rates**	**Pressure**
⊂⊃ 420°C	20 min	T° Stabilization + purge	
⊂⊃ 420°C	15 min	SiH_4 = 30 cc/min - O_2= 60 cc/min	200 mTorr
⊂⊃ 420°C	10 min	N_2 = 1 l/min (purge/vacuum)	1 Torr

⊂⊃ Depth measurement of diffused junction on test-wafer 1 - **Operation n°3 (§ XIX)**
⊂⊃ Thickness measurement {oxide diffusion e_d + LTO oxide e_n} on test-wafer 2 using profilemeter - **Operation n°4 (§ XIX)**
⊂⊃ Deduce LTO oxide e_n thickness

XII- PHOTOLITHOGRAPHY n° 3 : "CONTACTS OPENING"

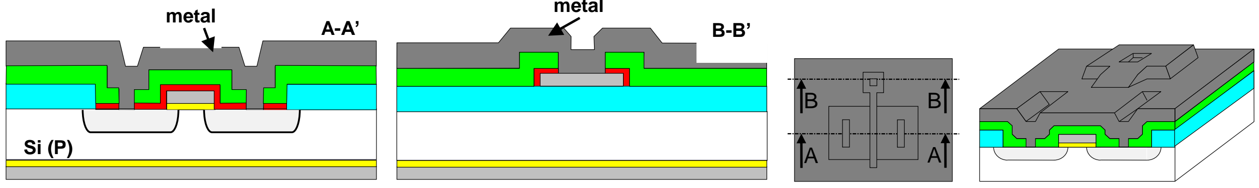


Operations	Conditions	Supervisor's visa for the continuation of Operations
⊂⊃ 1°) Drying	Hot plate 120°C – 2 min	
⊂⊃ 2°) HMDS deposit (Adhesion promoter)	Spin coater 4000 rpm - 30 s	
⊂⊃ 3°) Deposit resist	Resist Shipley S1813 Spin coater 4000 rpm - 30 s	
⊂⊃ 4°) 1st annealing	Hot plate 100°C – 60 s	
⊂⊃ 5°) Alignment - Insolation	Mask n°3 – 5 s	
⊂⊃ 6°) Development	Bath à 20 °C - 35 s	
⊂⊃ 7°) Rinsing	DI water	
⊂⊃ 8°) Drying	Spin dryer	
⊂⊃ 9°) Observation	Optical microscope	☐
⊂⊃ 10°) 2nd annealing	Hot plate 120° C - 45 s	
⊂⊃ 11°) SiO_2 etching	BOE HF : time duration given by test-wafer2	
⊂⊃ 12°) Rinsing	DI water	
⊂⊃ 13°) Drying	Spin dryer	
⊂⊃ 14°) Observation	Optical microscope	☐

⊂⊃ 15°) Resist dissolution	Acetone
⊂⊃ 16°) Rinsing	DI water
⊂⊃ 17°) Drying	Spin dryer
⊂⊃ 18°) Bring the components wafer to AIME staff for mounting on the sample holder	

⊂⊃ POLYSILICON thickness measurement on test-wafer 2 - **Operation n°5 (§ XIX)**

XIII- METALLIZATION



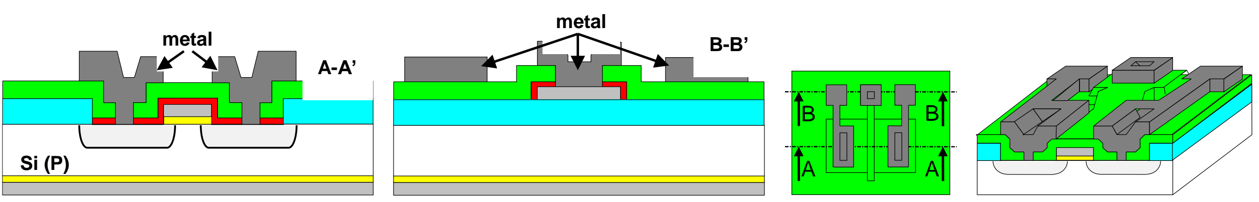
A 300 nm thick Aluminium layer is deposited on the wafer in this step.

Either by RF magnetron sputtering	⊂⊃ Deposit	Pressure before Deposit = 10^{-7} mbar Pressure during Deposit = 2.10^{-3} mbar Power RF = 150 W Target-substrate distance = 90 mm Duration of the Deposit = 15 min

OR

by thermal evaporation	⊂⊃ Degassing	T(subst.) = °C Duration = min
	⊂⊃ Deposit	Pressure before Deposit = mbar Pressure during Deposit = mbar

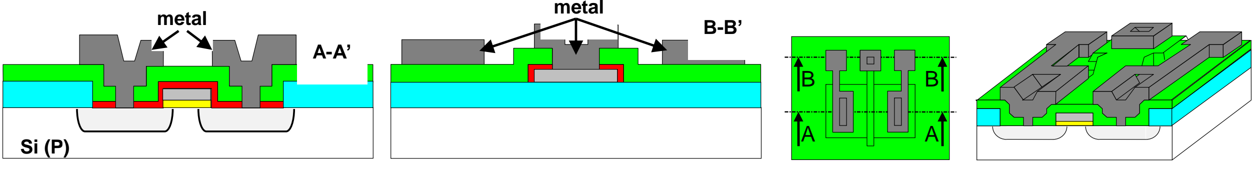
XIV- PHOTOLITHOGRAPHY n° 4 : "METAL ETCHING"



Supervisor's visa for the continuation of Operations		▼
Operations	**Conditions**	
⊂⊃ 0°) Aluminum etching bath homogenization.	Switch on the ultrasonic cleaner containing the Al etching bath.	

⊂⊃ 1°) Drying	Hot plate 120°C – 2 min	
⊂⊃ 2°) Resist deposit	Resist Shipley S1813 Spin coater 4000 rpm - 30 s	
Supervisor's visa for the continuation of Operations		▼
⊂⊃ 3°) 1st annealing	Hot plate 100°C – 60 s	
⊂⊃ 4°) Alignment - Insolation	Mask n°4 – 5 s	
⊂⊃ 5°) Development	Bath à 20 °C - 25 s	
⊂⊃ 6°) Rinsing	DI water	
⊂⊃ 7°) Drying	Spin dryer	
⊂⊃ 8°) Observation	Optical microscope	
⊂⊃ 9°) 2nd annealing	Hot plate 120° C - 45 s	
⊂⊃ 10°) Bath of Al etching	Stop the ultrasonic cleaner, and take out the Al etching bath	
⊂⊃ 11°) Al ETCHING	Al etching bath (40vol. H_3PO_4 + 7vol. HNO_3 + 7vol. H_2O) using **final control with naked eye** + 30 s of supplementary etching	
⊂⊃ 12°) Rinsing	DI water	
⊂⊃ 13°) Drying	Spin dryer	
⊂⊃ 14°) Observation	Optical microscope	

This photolithography is followed by the oxide etching of the backside of the components wafer.



Supervisor's visa for the continuation of Operations		▼
⊂⊃ 15°) Front side protection	UV film	
⊂⊃ 16°) POLYSILICON ETCHING backside	POLYSILICON etching bath (1vol.**HF** + 71vol.HNO_3 + 28vol.H_2O) using **final control with naked eye** : homogeneous grey color in the bath	
⊂⊃ 17°) De-oxidation backside	BOE HF (attaque SiO_2 grille) using **final control with naked eye** checking the hydrophobicity of the backside	
⊂⊃ 18°) Rinsing	DI water	
⊂⊃ 19°) Drying	Spin dryer	
⊂⊃ 20°) UV film glue degradation	UV Light– 5 min	
⊂⊃ 21°) Cleaning resist (2 faces)	Acetone	

⊂⊃ 22°) Rinsing	DI water
⊂⊃ 23°) Drying	Spin dryer

XV- METAL ANNEALING

This Operation is carried out in oven n ° 3-2 according to the conditions:

Temperature	Duration	Flow rates
⊂⊃ 400°C	20 min	$N_2 + H_2$ (5%)= 1 l/min

⊂⊃ Aluminum thickness measurement on "components" wafer using the profilemeter
⊂⊃ Fill in the 1st part of the results sheet before the wafer probing test

XVI- WAFER PROBING

⊂⊃ Quickly map the wafer to determine the region where the best components are located and select them.

XVII- ASSEMBLY

⊂⊃ DICING of the “components” wafer with a diamond blade
⊂⊃ MOUNTING on base: welding by gold-silicon eutectic at T = 370 ° C
⊂⊃ MICRO-WELDING by ultrasound (wedge bonding of Al-Si wire 5%, ∅ 25µm)

XVIII-ELECTRICAL TEST

See "characterization" pages

1°) - Measurement I(V) :

⊂⊃ Trace the I_D (V_{DS}) characteristics of a long channel transistor
⊂⊃ Trace the I_D (V_{GS}) characteristics of a long channel transistor
⊂⊃ Trace the I_D (V_{DS}) characteristics of a short channel transistor
⊂⊃ Trace the I_D (V_{GS}) characteristics of a short channel transistor
⊂⊃ Plot the characteristic I (V) of the diode

2°) - Measurement C(V) :

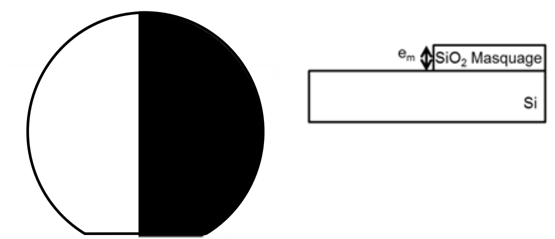
⊂⊃ Plot the characteristic C = f (V) of the MOS capacitance

XIX- OPERATIONS ON THE TEST WAFER

TEST WAFER **1:**

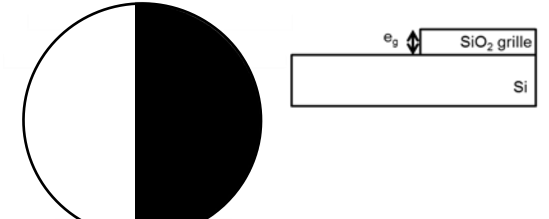
Operation n°1 :

During PHOTOLITHOGRAPHY n ° 1, Process test-wafer n ° 1 as in the figure opposite, that is to say:
a - Place a UV film on the right half of the wafer
b - Immerse the wafer in the BOE HF by measuring with precision the time necessary for the attack of the SiO_2.
NB – When all the characterizations have been carried out on the witness, the latter can be completely deoxidized (if possible, during the attack on the component platelets).



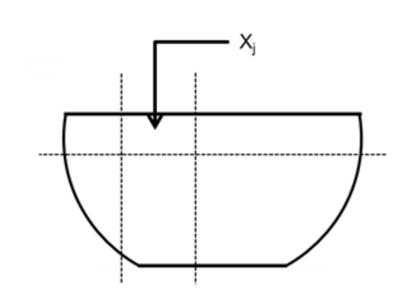
Opération n°2 :

a- Place a UV film on the right half of the wafer
b - Immerse the wafer in the BOE HF by measuring with precision the time necessary for the attack of the SiO_2.
NB – When all the characterizations have been carried out on the witness, the latter can be completely deoxidized (if possible, during the attack on the component platelets).



Operation n°3 :

During the Deposit SiO_2 L.T.O., Process test-wafer n ° 1 as in the figure opposite, that is to say:
a - measure the thickness of the diffusion oxide with an ellipsometer.
b - immerse the test-wafer in the BOE HF (approximately 1mn) to remove the SiO_2 created during the diffusion.
c - cut a square of about 9 mm and make a lapping with a roller + diamond paste, then rinse and dry.
d - put a flat drop of developer on the lapping and observe under the microscope, then blow-dry when the diffused junction appears.
e - measure the scattered junction depth “Xj” under the microscope and with the form.



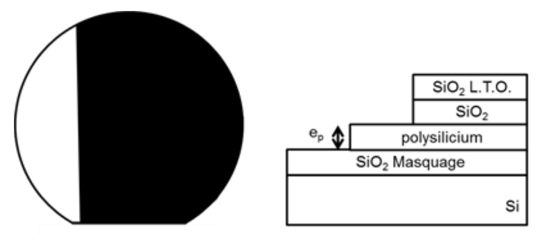
TEST WAFER **2 :**

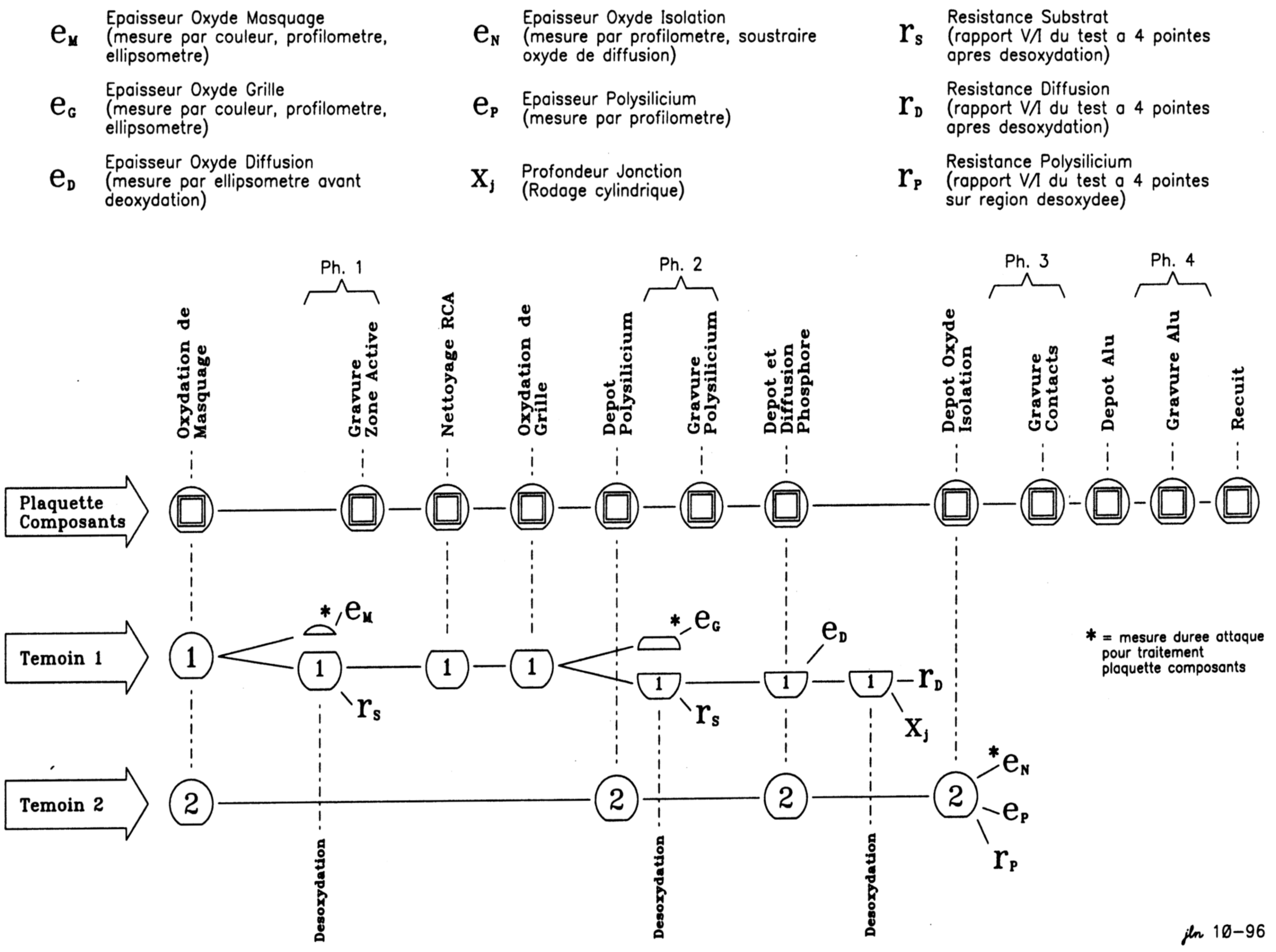
Operation n°4 :

During PHOTOLITHOGRAPHY n ° 3, Process test-wafer n ° 2 as in the figure opposite, that is to say:
a - Place a UV film on the right half of the small piece;
b - immerse the test-wafer in the BOE HF by measuring with precision the time necessary for the attack of the SiO_2.

Operation n°5 :

During PHOTOLITHOGRAPHY n ° 3, Process test-wafer n ° 2 as in the figure opposite, that is to say:
a - Place a UV film on the right half of the small piece (cover the previous step);
b - immerse the test-wafer in the POLYSILICON etching bath (attack completed when the color is homogeneous grey: we then see the silicon under the SiO_2 which is colorless in the bath).





eM Epaisseur Oxyde Masquage (mesure par couleur, profilometre, ellipsometre)
eG Epaisseur Oxyde Grille (mesure par couleur, profilometre, ellipsometre)
eD Epaisseur Oxyde Diffusion (mesure par ellipsometre avant deoxydation)
eN Epaisseur Oxyde Isolation (mesure par profilometre, soustraire oxyde de diffusion)
eP Epaisseur Polysilicium (mesure par profilometre)
Xj Profondeur Jonction (Rodage cylindrique)
rS Resistance Substrat (rapport V/I du test a 4 pointes apres desoxydation)
rD Resistance Diffusion (rapport V/I du test a 4 pointes apres desoxydation)
rP Resistance Polysilicium (rapport V/I du test a 4 pointes sur region desoxydee)
Ph. 1
Ph. 2
Ph. 3
Ph. 4
Oxydation de Masquage
Gravure Zone Active
Nettoyage RCA
Oxydation de Grille
Depot Polysilicium
Gravure Polysilicium
Depot et Diffusion Phosphore
Depot Oxyde Isolation
Gravure Contacts
Depot Alu
Gravure Alu
Recuit
Plaquette Composants
Temoin 1
Temoin 2
Desoxydation
Desoxydation
Desoxydation
* = mesure duree attaque pour traitement plaquette composants
jln 10–96

XX- CHARACTERIZATIONS

I- SUBSTRATE CHARACTERIZATION:

At the start of the process, we measure:

- the four points measurement : V/I = ... Ω
- the thickness of the slices: e_s = ... µm

We deduce:

→ $R_{\square s}$ = ... Ω

→ ρ_s = ... Ω.cm

→ N_A = ... at/cm^3

II - MEASUREMENTS OF OXIDE THICKNESSES:

a- Masking oxide after Operation II e_m = ... µm

b- Gate oxide after Operation VI e_g = ... µm

c- Diffusion oxide after Operation X e_d = ... µm

d- L.T.O. after Operation XI e_n = ... µm

III- CHARACTERIZATION OF THE DIFFUSION:

After step X (diffusion of the substrate), Measurements of :

V/I = ... Ω → $R_{\square d}$ = ... Ω

X_j = ... µm → ρ_d = ... Ω.cm

→ C_s = ... at /cm3

IV- CHARACTERIZATION OF THE DOPED POLYSILICON LAYER:

After step X (diffusion of the substrate), Measures of :

V/I = ... Ω → $R_{\square p}$ = ... Ω

e_p = ... µm → ρ_p = ... Ω.cm

V- ELECTRICAL TESTS:

The list of measurements mentioned below is given by way of example to allow either comparisons with theoretical values or the determination of new technological parameters.

1 - For each of the transistors of a chip:

⊂⊃ Trace the network of characteristics I_D (V_{DS}) and I_D (V_{GS}) and deduce

- • g_m transconductance
- • the on-state resistance R_{on} (for V_{GS} = 5 V)[1]

⊂⊃ We can also evaluate:

- Current I_{DS0} at V_{GS}= 0
- the threshold voltage V_T
- the breakdown voltage V_B

To be able to do the calculations, it is necessary to know the geometric dimensions of the components produced:

Transistor MOS "long channel"		
L = ...µm - W = ...µm		
g_m = ...mS	R_{on} = ...Ω	
V_T =..............V	V_B =..............V	I_{DS0} =..........µA

Transistor MOS "short channel"		
L = ...µm - W = ...µm		
g_m = ...mS	R_{on} = ...Ω	
V_T =..............V	V_B =..............V	I_{DS0} =..........µA

2 – For the MOS capacitor:

⊂⊃ Draw the curve C (V) in high frequencies and deduce from it C_{ox}, C_{dep}, V_T et Q_{SS} :

MOS Capacitor : S = cm^2	
C_{ox} = ...pF	e_{ox} = ...µm
C_{dep} = ...pF	
V_T = ...V	N_{ox} =..charges.cm^{-2}

[1] The experimental value R_{on} is obtained by measuring the slope of the characteristic $I_D(V_{DS})$à V_{GS} = constant in the region where the current increases linearly with the voltage.

XXI- MEASUREMENT OF JUNCTION DEPTHS

DEFINITION:
Xj is the distance counted from the silicon surface such that C (Xj) = C_B
C (x) corresponding to the doping profile of the diffused zone and C_B to that of the substrate.

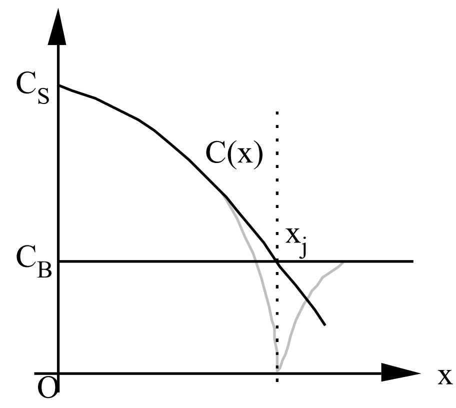


Figure 1

PROCEDURE:
a- Mechanical digging of the sample by a cylinder of radius R coated with diamond paste to obtain an imprint with a depth greater than Xj.

b- Chemical revelation which colors the N zone and the P zone differently.

c- Observation under Optical microscope and measurement of quantities x and y (fig. 3).

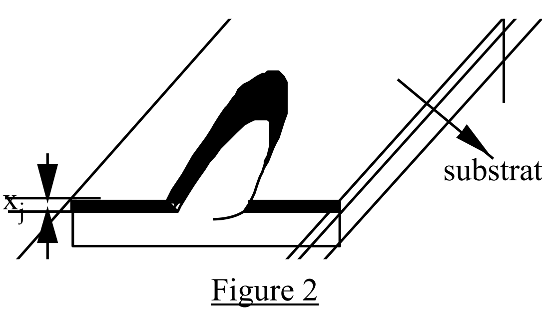


Figure 2

CALCULATION OF X_J :
With the notations in the figure, the measured lengths x and y are such that:

$$\left.\begin{array}{l} x = a - b \\ y = a + b \end{array}\right\} \quad xy = a^2 - b^2$$

In addition, simple geometric considerations lead to:

$$x_j = \{R^2 - b^2\}^{\frac{1}{2}} - \{R^2 - a^2\}^{\frac{1}{2}}$$

$$8 \;\; R \left\{\left(1 - \frac{b^2}{2R^2}\right) - \left(1 - \frac{a^2}{2R^2}\right)\right\} = \frac{xy}{2R}$$

$$= \frac{xy}{2R}$$

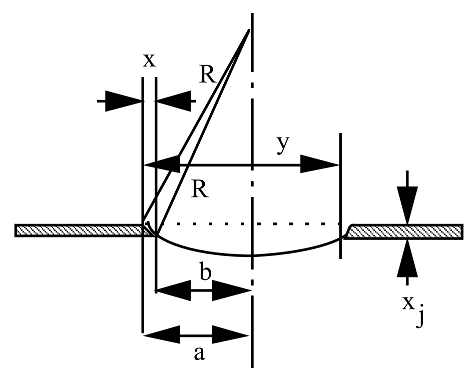


Figure 3

Taking into account the radius of the cylinder R = 1.25 cm and the magnification of the microscope, we have:

objective X 3,2 1 division of Vernier screw → 1 µm and

$$\boxed{x_j\,(\mu m) = 39{,}9 \;.\; 10^{-6} \;\; x_{(div)} \cdot y_{(div)}}$$

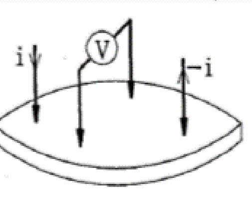
objective X 5 1 division of Vernier screw→ 0,6 µm and

$$\boxed{x_j\,(\mu m) = 14{,}40 \;.\; 10^{-6} \;\; x_{(div)} \cdot y_{(div)}}$$

XXII- 4-POINT RESISTIVITY MEASUREMENT

Measure 4 points

1. V/I measurement on a thin layer of thickness and resistivity ρ



If the thickness is negligible compared to the other dimensions, we can construct a two-dimensional model of the conduction which women:

$$\frac{V}{I} = K \cdot \frac{\rho}{e} \quad (1)$$

Kbeing a dimensionless coefficient characteristic of 2D geometry (shape of contours, position of contacts).

The ρle ratio characterizes the layer, we note it R. We then have: $\frac{V}{I} = K \cdot R_{\square}$ (2)

(N.B. $R_{\square}$ is expressed in Ohms)

2. Value of K (special case)

The coefficient K can be calculated analytically in some very simple particular cases, for example for 4 points aligned equidistant on a layer without limits (infinite):

$$K = \frac{\log(2)}{\pi} \quad (3)$$

(practical value: 1/K = 4.532)

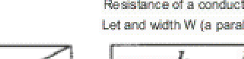
3. Case of a doped layer

The resistivity is not uniform over the thickness e, but formals (2) and (3) are still applicable, by generalization of the use of Ro

We then define an average resistivity Pm such that: Ra = $\frac{\rho_m}{e}$ (4)

If the dopant distribution law is known, Pla concentration can be deduced at the surface and for different depths (see charts).

4. Relationship with mask drawing



Resistance of a conductive track of length Let and width W (a parallelepiped):

$$R = \rho \cdot \frac{L}{S} = \rho \cdot \frac{L}{eW} = \frac{L}{W} \cdot R_{\square} \quad (5)$$

where Let W characterizes the design of the masks while R characterizes the technology. The L/W ratio can be considered as a "number of squares", hence the name Ro: "resistance per square".

5. Case of significant thickness

If the thickness of the layer is not negligible but still reasonably small, formulas (2) and (3) can be applied by replacing K by a corrected K coefficient, a function of the ratio between the thickness and the other dimensions.

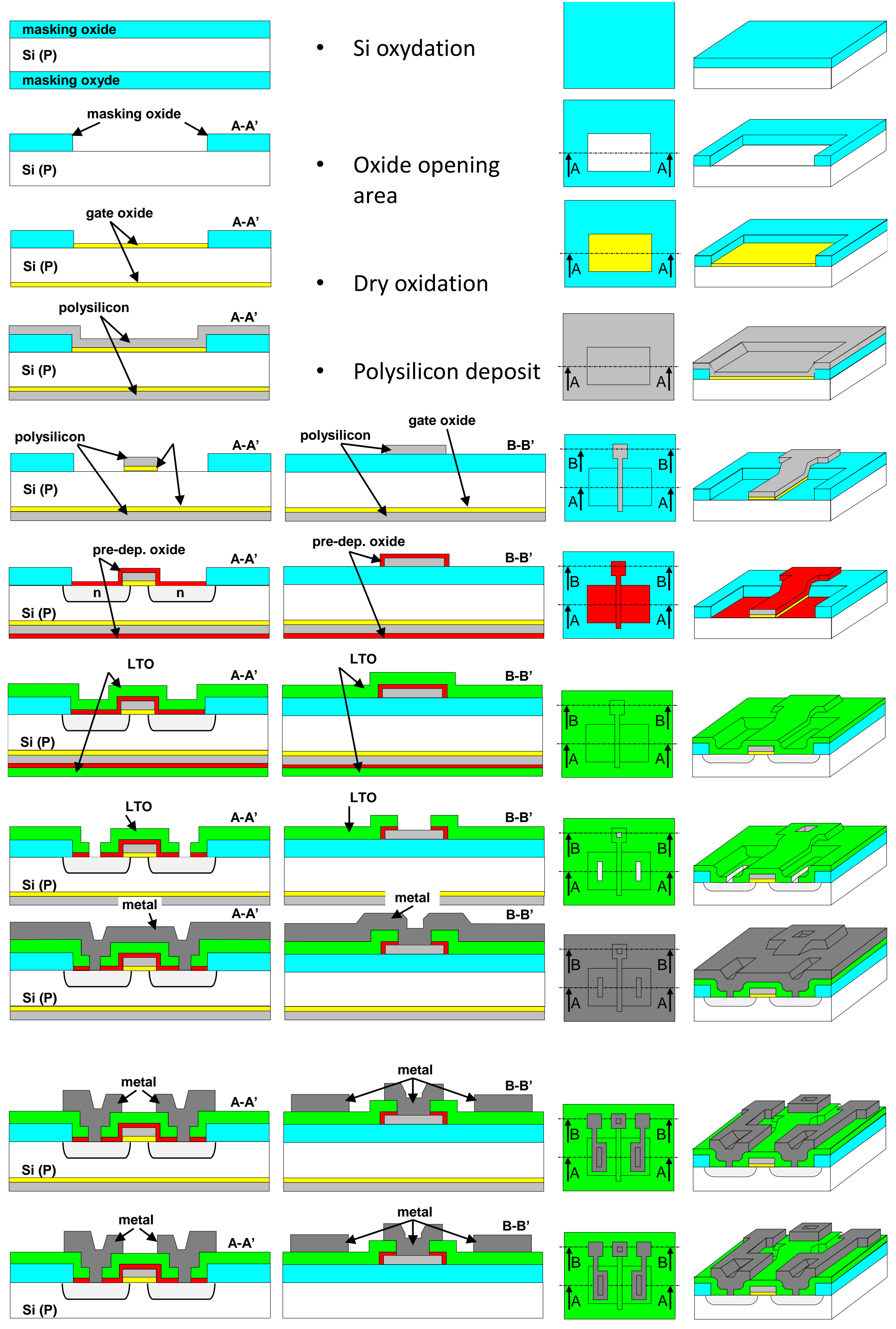
In the case of the 4 equidistant points of distance d, the correction is negligible as long as:

$$\frac{e}{d} < 0.25$$

Practical method for measuring 4 points:

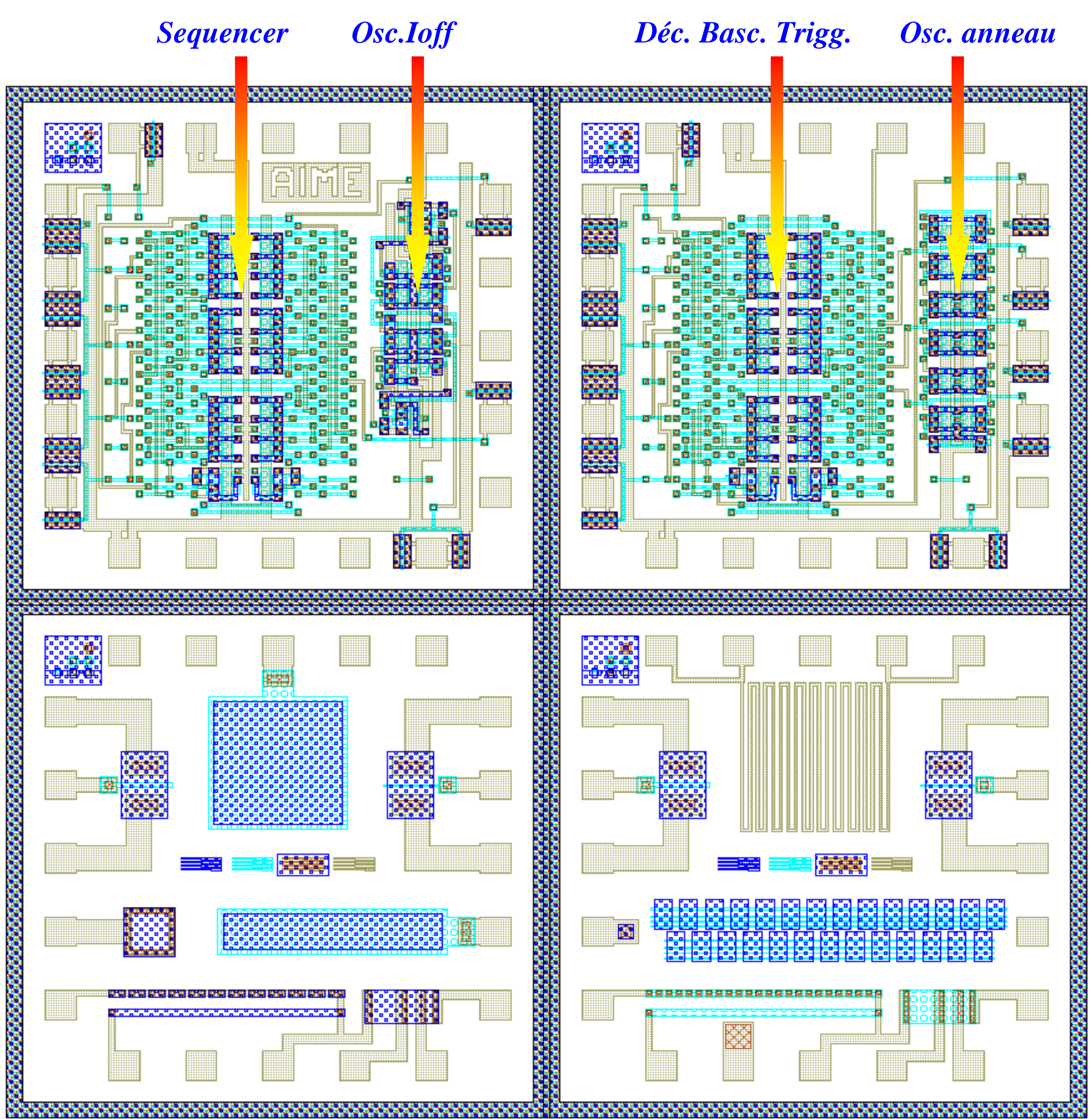
- perform a V/I measurement not too close to the edges of the sample
- express the measurement in Ohms
- multiply by 4.532 to obtain R, note this result (always in Ohms)
  (the distance between points being 1.59 mm, the thickness correction is not necessary)
- express the thickness of the layer in cm.
- multiply Ropar e to obtain the resistivity for Pm note this result (in
- Ohm.cm) use an abacus to deduce the dopant concentration (after possibly calculation of conductivity in Ohm⁻¹.cm⁻¹).
  ATTENTION: it is not the same chart depending on whether the doping is uniform (substrate, deposited polysilicon) or not (diffused or implanted layer).

XXIII-SECTIONAL VIEWS OF THE DIFFERENT STAGES OF THE PROCESS



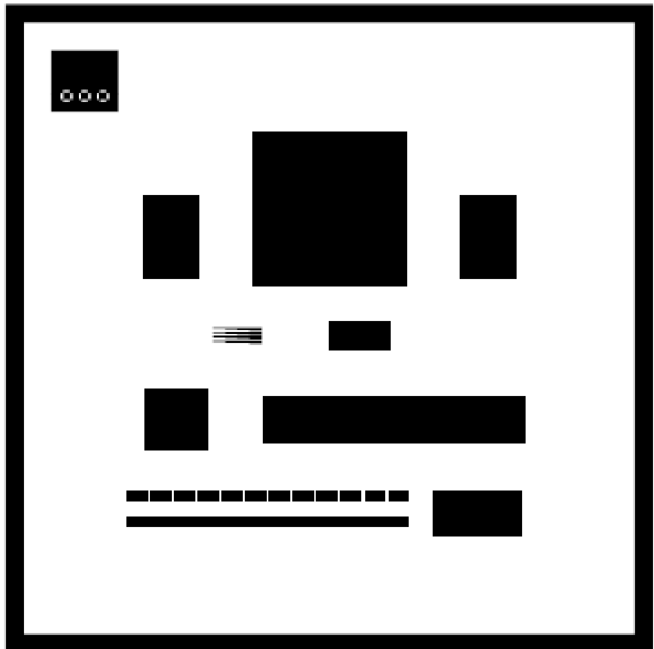
XXIV-SET OF MASKS DTC4R

CHIP C3 **CHIP C4**

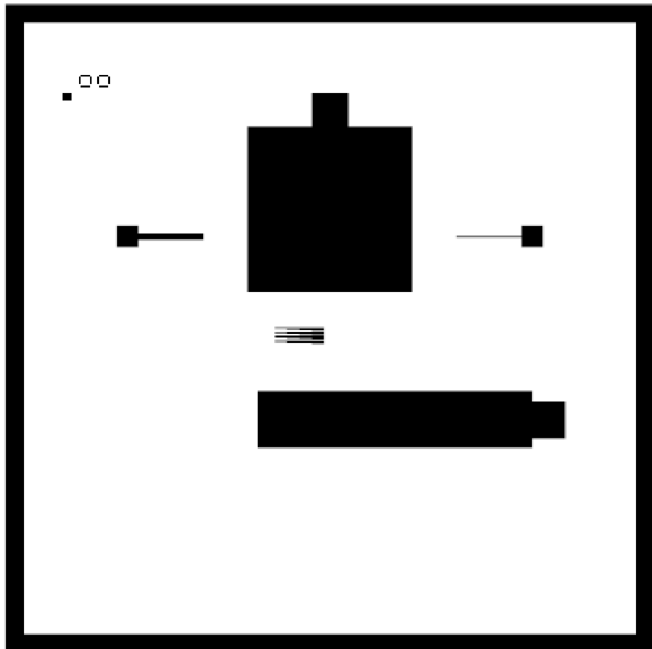


CHIP C1 **CHIP C2**

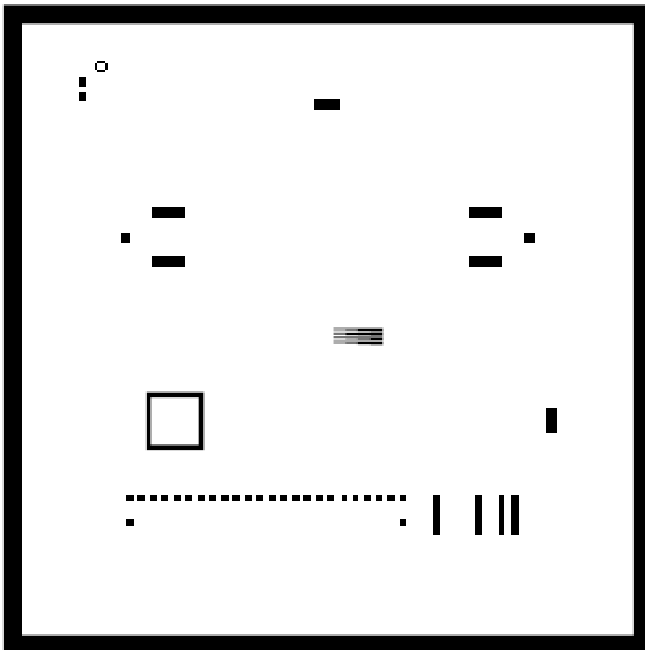
DTC4R : CHIP C1



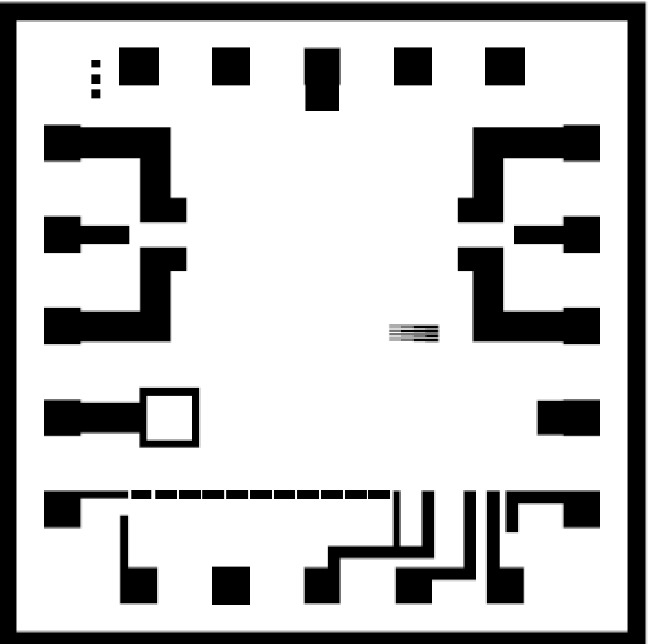
NIV. 1 : Zone Active



NIV. 2 : Polysilicum

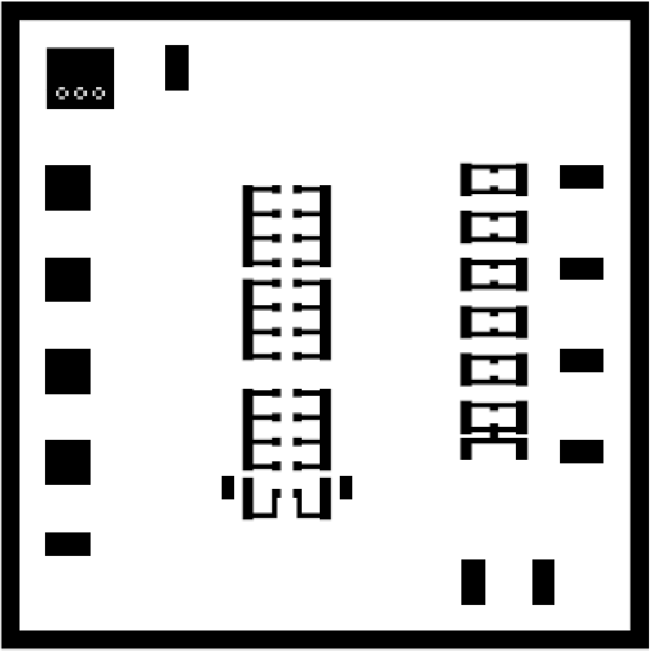


NIV. 3 : Contact

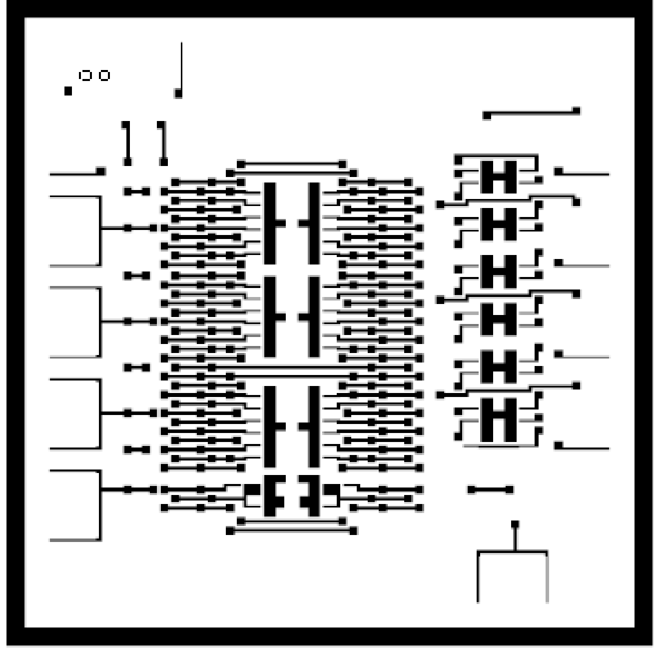


NIV. 4 : Alu

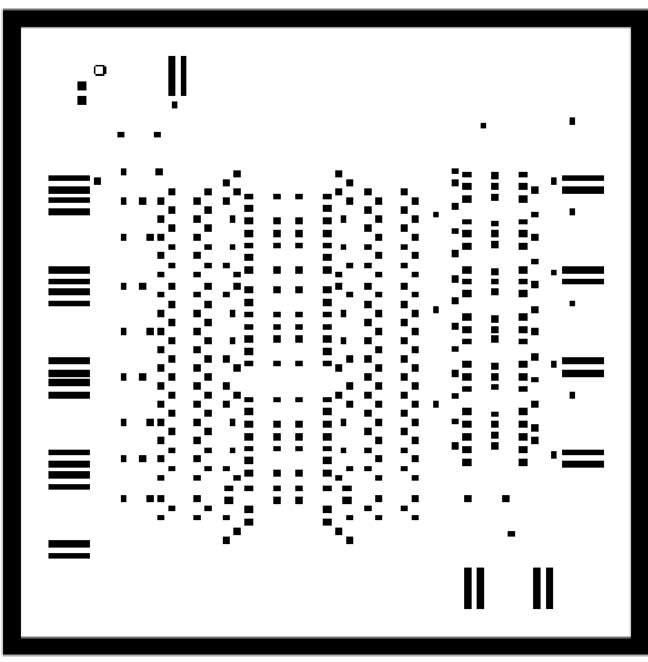
DTC4R : CHIP C4



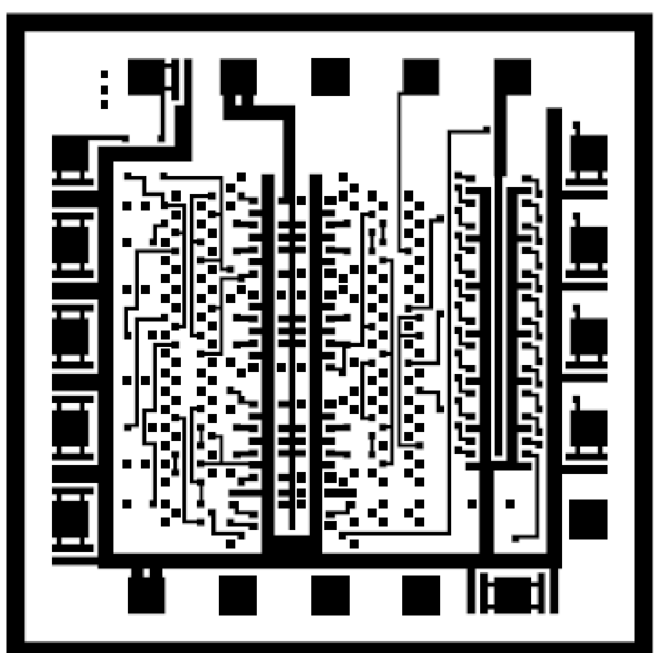
NIV. 1 : Zone Active



NIV. 2 : Polysilicum



NIV. 3 : Contact



NIV. 4 : Alu

XXV- FORMS FOR ELECTRICAL TESTS

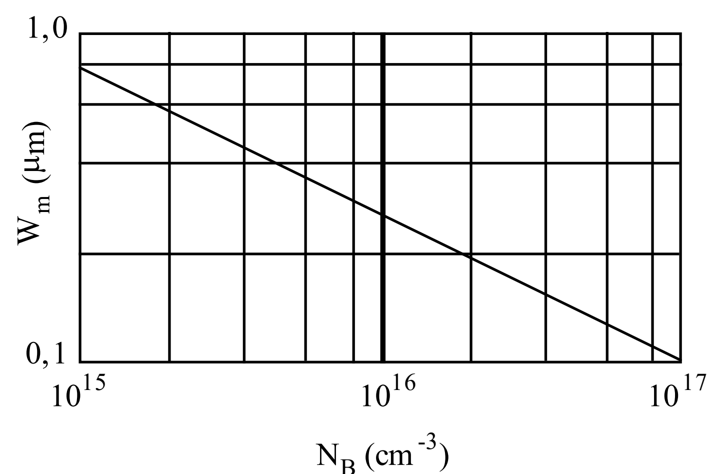
I- MOS CAPACITOR (Substrate P, High frequency Measurement (1 MHz))

$$C_{MAX} = C_{OX} = S \frac{\varepsilon_o \varepsilon_{OX}}{e_{OX}}$$

$$\frac{1}{C_{MIN}} = \frac{1}{C_{OX}} + \frac{1}{C_{dep}}$$

$$C_{dep} = S \frac{\varepsilon_o \varepsilon_{Si}}{W_{MAX}}$$

$$W_{MAX}^2 = \frac{kT}{q} \frac{4 \varepsilon_o \varepsilon_{Si}}{qN_A} \log\left(\frac{N_A}{n_i}\right)$$



II- TRANSCONDUCTANCE OF A MOS TRANSISTOR (saturated regime)

$$g_m = \frac{Z}{L} \mu_n \frac{\varepsilon_o \varepsilon_{OX}}{e_{OX}} (V_G - V_T) \quad \rightarrow \quad Z \frac{\varepsilon_o \varepsilon_{OX}}{e_{OX}} v_s$$

III- THRESHOLD VOLTAGE (channel N)

$$V_{T\,mes} = V_{T\,id} - \frac{Q_{SS}}{C_{OX}} \quad \text{ou} \quad N_{SS} = (V_{T\,mes} - V_{T\,id}) \frac{C_{OX}}{q\,S} \; (cm^{-2})$$

et $$V_{T\,id} = \Phi_{ms} + 2\,\Phi_F + \; + \sqrt{2\,\Phi_B\,\Phi_F}$$

avec $$\Phi_B = 2\; N_A \frac{e_{OX}^2}{\varepsilon_o\,\varepsilon_{OX}} \frac{\varepsilon_{Si}}{\varepsilon_{OX}} \qquad \Phi_F = \frac{kT}{q} \mathrm{Log} \frac{N_A}{n_i}$$

$$\Phi_{ms} = \Phi_m - \left(X_{si} + \frac{Eg}{2q} + \Phi_F\right)$$

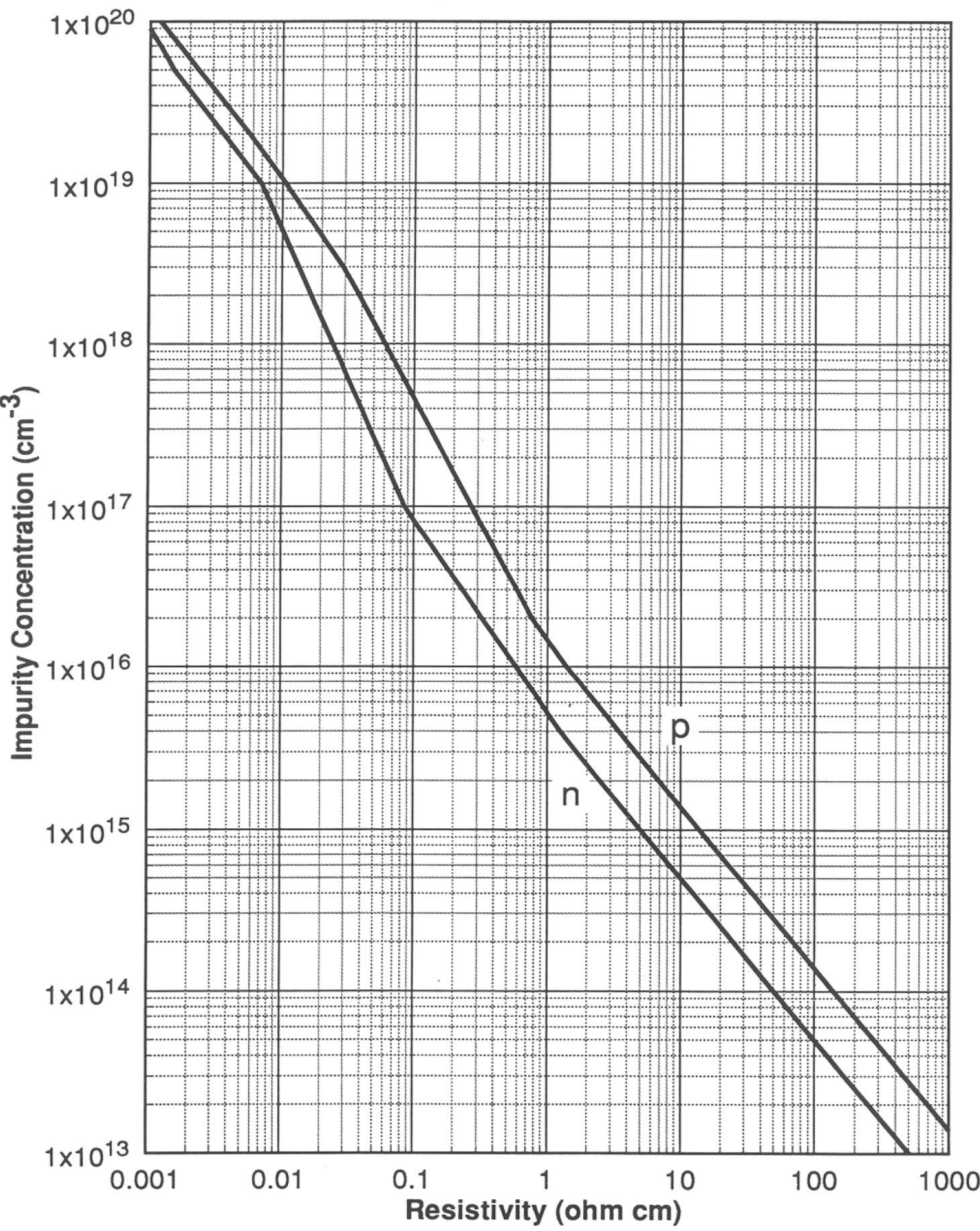
IV- SOME NUMERICAL VALUES (Si, T = 300 °K)

$U_T = \frac{kT}{q} = 0{,}0259$ V ; $\frac{E_g}{2q} = 0{,}56$ V ; $n_i = 1{,}45 \,.\, 10^{10}$ cm^{-3}

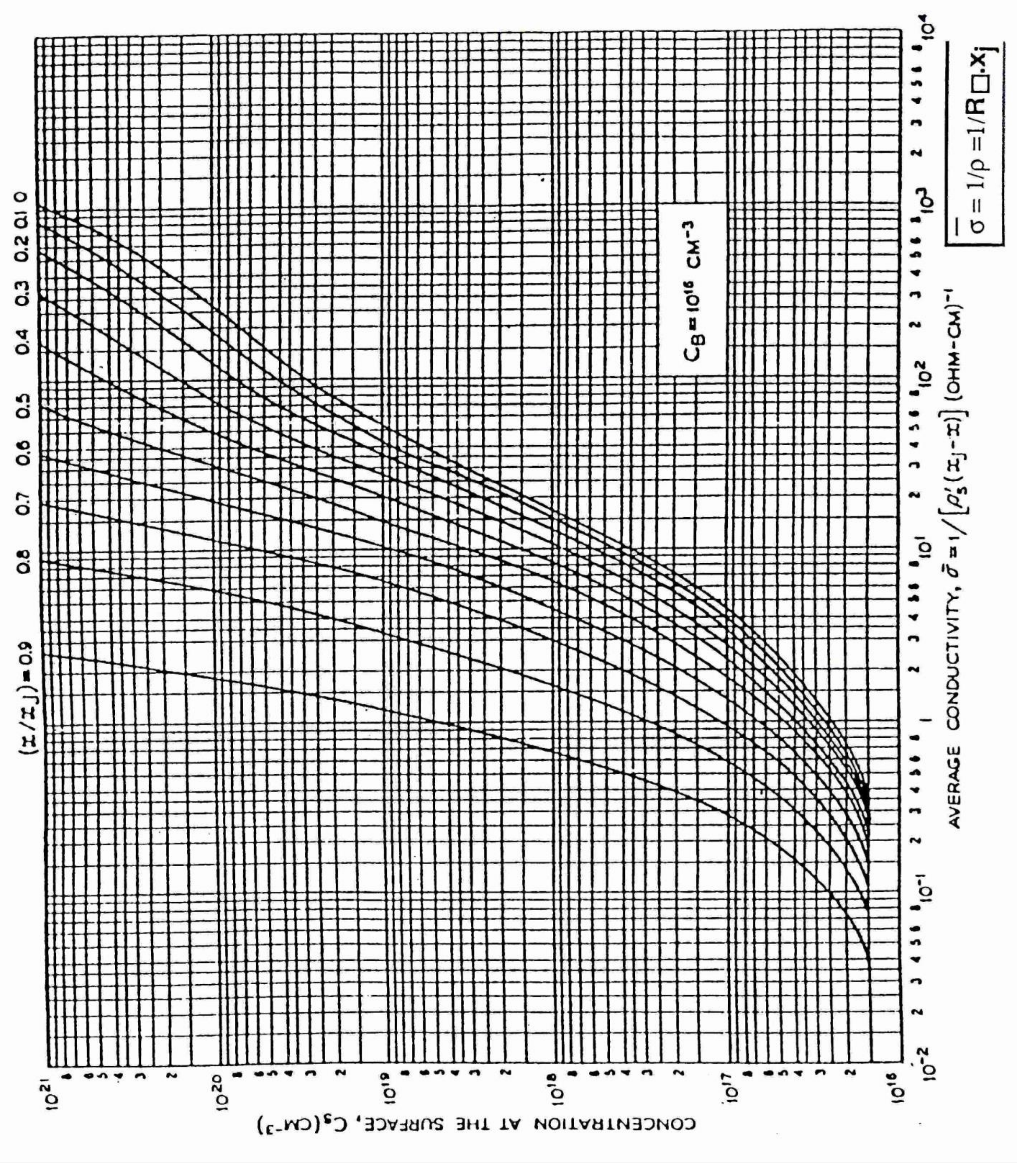
$\varepsilon_{Si} = 11{,}9$; $\varepsilon_{OX} = 3{,}9$; $\varepsilon_o = 8{,}85 \,.\, 10^{-14}$ F.cm^{-1} ; $v_s = 10^7$ cm.s^{-1}

Pour une grille en Al : $\Phi_m - x_{Si} = -\,0{,}11$ V

V- SILICON DOPING



VI- DOPING OF DIFFUSED LAYERS AFTER PREDEPOSITION



I Theoretical calculation of the threshold voltage V, of the MOS

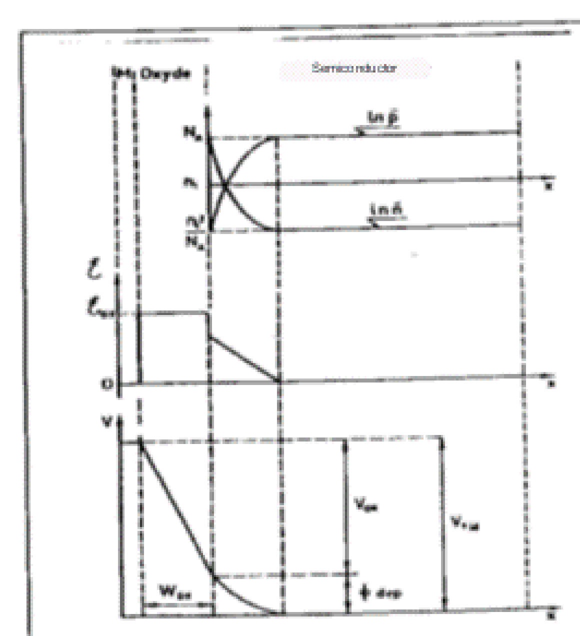
Notations

- Wo and Wsi work on grid output and the S, respectively.
- $\phi_{ms} = \frac{\text{Wo-Ws}}{q}$ equivalent voltage of the output work difference
- ϕ dep: tension supported by the depopulated zone of thickness Wdep max
- AVox: voltage supported by the gate oxide at threshold.
- Qss: charge in C/cm² in the oxide (negative charge in the channel)
- Nss $= \frac{Q_{ss}}{q}$ equivalent in atoms/cm²
- eox- gate oxide thickness
- Cox =εox/eox Capacity of gate oxide per unit area

☐ threshold voltage V,VT + V must be >0 in the NMOS

☐ VFB: negative flat band voltage

$$V_{FB} = \frac{W_G - W_{Si}}{q} - \frac{Q_{SS}}{C_{OX}} < 0$$



Ideal case

ϕm0 and Qss-0

VTid AVox+dp>0 in NMOS

Pop-2UT ln $\frac{NA}{n_i}$

$$\Delta V_{ox} = \frac{e_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{Si}N_A\phi_{dep}}$$

About ϕ_{ms}

The following chart makes it possible to determine the difference in output work between ga and Si according to the type of substrate (N or P) and according to its doping and for variou of gates (Poly SN, Poly S.P' or Al).

Ex : substrat P, $N_A=10^{16}$, Grille $N^+S_i \Rightarrow \phi_{ms} \cong -0,8V$

☐ Dielectric data

$\varepsilon_{OX}=3,9\ \varepsilon_0$

$\varepsilon_0=8,85.10^{-14}F/cm$

$\varepsilon_{Si}=11,9\ \varepsilon_0$

☐ Data S, at 300°K: intrinsic density $n_i=10^{10}cm^{-3}$

band gap : $Eg=1,12eV$

thermodynamic voltage $U_T=\frac{kT}{q}=26mV$

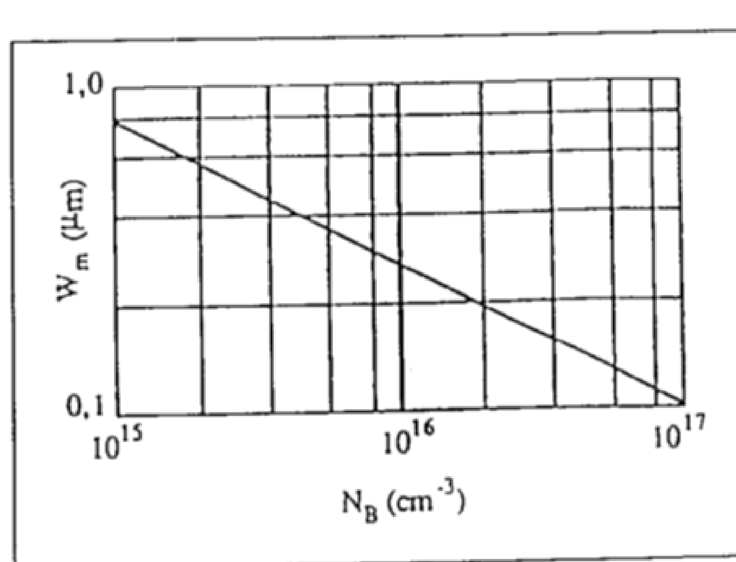
II MOS capacity (Substrate P, High frequency measurements (1 MHZ))

$$C_{MAX}=C_{OX}=S\frac{\varepsilon_o\varepsilon_{OX}}{e_{OX}}$$

$$\frac{1}{C_{MIN}}=\frac{1}{C_{OX}}+\frac{1}{C_{dep}}$$

$$C_{dep}=S\frac{\varepsilon_o\varepsilon_{Si}}{W_{MAX}}$$

$$W_{MAX}^2+\frac{kT}{q}\frac{4\varepsilon_o\varepsilon_{Si}}{qN_A}\log\left(\frac{N_A}{n_i}\right)$$



III Transconductance of a MOS transistor (saturated mode)

$$g_m=\frac{Z}{L}\mu_n\frac{\varepsilon_o\varepsilon_{OX}}{e_{OX}}(V_G-V_T) \quad \rightarrow \quad Z\frac{\varepsilon_o\varepsilon_{OX}}{e_{OX}}v_s$$

ϕ_{MS} versus Silicon Doping for Various Gate Electrodes